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以不同模型技術評估雙閘極互補式金氧半場效電晶體的電路效能

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摘　　要

此論文主要是探討雙閘極互補式金氧半場效電晶體模型技術，其應用範圍在於元件與電路的模擬。這些模型技術包括了查表模型、精簡模型及混合式模擬，各種模型技術各有其特色。我們運用了不同的模型技術來評估雙閘極互補式金氧半場效電晶體的電路效能，並且在電路應用的設計上，提供了最佳化的設計方法。

關鍵字：雙閘極金氧半場效電晶體，鰭式場效電晶體，TCAD，精簡模型

On the Evaluation of Double-Gate CMOS Circuit Performance via Different Modeling Techniques

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Abstract

Double-gate CMOS modeling techniques for device and circuit simulations are presented. The modeling techniques, including look-up table modeling, compact device modeling, and mixed-mode simulation, have their unique features suitable for evaluating high performance Double-Gate CMOS circuits.

Keywords： Double-Gate MOSFET, FinFET, TCAD, compact model.

I. Introduction

Interest in the double-gate (DG) MOSFET has been growing as the end of the ITRS roadmap [1] is being approached, the conceptual figure of which is shown in Fig. 1. The inherent gate-gate charge coupling via the thin Si film effectively reduces short-channel effects (SCEs) and yields higher drive current [2]. The novel DG device retains the advantages of the FD/SOI MOSFET, and is highly scalable, unlike the FD/SOI device, which is plagued by underlying BOX fringing fields and associated SCEs [3]. In order to study and analyze DG CMOS devices and circuits comprehensively, a robust and reliable modeling technique is needed.

Several modeling techniques are applicable to DG CMOS, including look-up table (LUT) modeling [4], compact device modeling [5-7], and mixed-mode simulation [8]. The LUT modeling can be quickly done based on a developed device technology. The models are constructed from the results of device simulations, covering the entire bias range for the projected application. On the other hand, the development of the compact model requires solid understanding of device physics and involves proper approximations of sophisticated analytical equations. Hence, it usually takes years to complete the model through numerous refinements. However, once it is available via the circuit simulator, e.g., SPICE, it can be intensively used for large-scale circuit simulation. Last, the mixed-mode simulation, assisted by device simulator, is somewhat similar to LUT model but without the necessity of pre-simulation for model generation. It is convenient for quick assessment of a developed device technology. However, its simulation time could be lengthy, depending on the size of the circuit and/or the simulated condition. The examples for these modeling techniques are reviewed in following sections, respectively.

II. Look-up table modeling

The methodology of LUT modeling is shown in Fig. 2. Herein we demonstrate an example of LUT modeling applied to FinFETs [4] [9]. A FinFET is a DG transistor, as plotted in Fig. 3, having surface conduction channels on two opposite vertical surfaces and current flowing in the horizontal direction. Both fin (silicon wall) width and channel length are usually determined by a lithographic step.

Our LUT model is based on TCAD simulations taking into account process limitations in making a very thin silicon wall device. We use 5nm thick silicon channel, and source and drain regions are fanned out into a fully silicided layer in order to minimize parasitic resistance. To compare FinFET with single-gate device we also create an FDSOI device with the same channel thickness of 5nm and adjust I_{off} by modifying gate work function. Capacitive coupling of the FinFET device with the substrate beneath the buried oxide has been neglected. Gate material is chosen to achieve off-state leakage of 1μA/μm for both NMOS and PMOS devices.

At higher V_{dd} FinFET shows ideal subthreshold slope and 15 mV/V DIBL compared to 87 mV/dec slope in linear and 106mV/dec slope in saturation regime, and 175 mV/V DIBL for FDSOI device, as indicated in Fig. 4. Even for low power supply (0.4 V) FinFET shows excellent subthreshold slope (65 mV/dec) and 50 mV/V DIBL, while the subthreshold slope of FDSOI remains high and DIBL becomes really bad (280 mV/V), which will affect AC performance. For FinFET we assume a 50 nm fin height and each fin contributes twice that amount toward device

width.

In our simulations we use three different V_{dd}'s (0.4, 0.6, and 0.8 V). We compare nine-stage inverter ring oscillator having devices with fixed I_{on} (3 mA) by adjusting width for NMOS and PMOS respectively. FinFET shows great performance for low operating voltages (~30% better than single-gate) since ideal subthreshold slope enables larger gate overdrive, as shown in Fig. 5. For higher operation voltages the performance enhancement shrinks to 7%. In Fig. 6, the power-delay curve suggests that better performance results in larger power consumption, and the single-gate devices show better power-delay product than FinFET for V_{dd} = 0.8 V.

FinFET layout differs from planar CMOS for wide devices. Width of a wide device is achieved by putting multiple fins in parallel between the source and drain (insert of Fig. 7). For 45 nm technology the fin pitch is expected to be 10-12 nm. If spacer technique [10] is used to form fins then half that pitch is possible. Minimizing the pitch can significantly improve available drive current per silicon area [11]. But wrapping the gate around multiple fins introduces a long piece of poly with a single gate contact thus causing significant gate resistance. The effect of distributed gate resistance is shown in Fig. 7. We can see that it is an imperative to achieve a smallest pitch possible. All advantages in performance over single-gate devices could be gone if fin design or process is not improved. Higher fins would benefit delays significantly, although they may not be practical for manufacturing due to a very high aspect ratio. For circuits with small width devices the penalty is much smaller, shown by the third curve in Fig. 7. The easiest solution for this problem would be putting multiple gate contacts but this would make circuit layout larger and is also circuit specific so it is very difficult to quantify it. From the presented examples, LUT modeling has demonstrated its usage for preliminary assessment of device performance at early stage.

III. Compact device modeling

In order to study and analyze DG CMOS devices and circuits comprehensively, a generic compact physical model is needed. Two types of DG MOSFETs are contemplated for future CMOS: symmetrical-gate and asymmetrical-gate (e.g., n^+/p^+ polysilicon gates) devices. The generic compact model [5-7], suitable for both types of DG MOSFETs, is useful for general purpose.

The operation of DG MOSFETs can be physically characterized in weak- and strong-inversion regions of operation via analyses that are applicable to compact modeling.

For weak inversion, a two-dimensional (2D) weak-inversion analysis [3], which accounts for back-channel current with the charge coupling between two gates, is applicable to the DG MOSFET. Hence, this model can be the initial basis for evaluating the channel current, which is obtained by integrating the predominant diffusion current over the entire Si film.

For an n-channel device, the model basically solves Poisson's equation applied to the intrinsic region of Si film [3],

$$\frac{\partial^2}{\partial x^2}\psi(x,y)+\frac{\partial^2}{\partial y^2}\psi(x,y)\cong\frac{q}{\varepsilon_s}N_A, \qquad (1)$$

based on the depletion approximation, where N_A is the channel doping density and ψ is the electrostatic potential in the Si film. With boundary conditions properly defined at the Si-SiO_2 interfaces and metallurgical junctions, an analytical solution of (1) can be obtained by assuming a second-order polynomial function for the electric potential. Also, the short-channel effects, such as DIBL and L-dependent subthreshold slope, can be implicitly predicted

from the 2D weak-inversion analysis. The derived potential is then used to model the subthreshold current, which is assumed to be predominantly diffusion along a modulated channel length, by integrating the current density over the entire Si film. The total weak-inversion current can be expressed as the sum of front- and back-channel components.

For strong inversion, the 1D Poisson's equation applied to the Si film between the gates,

$$\frac{dE}{dx} = -\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s}[p(x) - n(x) - N_A(x)], \quad (2)$$

could be solved numerically. Such solution would show

$$\int_0^{T_{Si}} E dx = \psi_{sf} - \psi_{sb} \quad (3)$$

where the front- and back-surface potentials ψ_{sf} and ψ_{sb} relate to the front- and back-gate voltages via

$$V_{GfS} = V_{FB}^f + \psi_{sf} + \frac{\varepsilon_s E_{sf}}{C_{of}} \quad (4)$$

and

$$V_{GbS} = V_{FB}^b + \psi_{sb} + \frac{\varepsilon_s E_{sb}}{C_{ob}}; \quad (5)$$

V_{FB}^f and V_{FB}^b are flatband voltages referenced to the (hypothetical) neutral body, C_{of} and C_{ob} are the front- and back-oxide capacitances, and E_{sf} and E_{sb} are the front- and back-surface electric fields. To get a compact model for strong inversion ($n >> N_A$), (2) can be approximated as

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s} n(x). \quad (6)$$

In writing (6), we have assumed a "volume inversion" condition [12], which allows carriers to be anywhere in the thin Si film (and which is consistent with the quantum-mechanical analysis). Multiplying both sides of (6) by $2(d\psi/dx)dx$ and integrating from the back surface to the front surface, we obtain

$$E_{sf}^2 - E_{sb}^2 = \frac{2n_i^2 kT}{\varepsilon_s N_A}[\exp(\frac{q\psi_{sf}}{kT}) - \exp(\frac{q\psi_{sb}}{kT})], \quad (7)$$

which provides a useful relationship between electric fields and surface potentials in an analytical form. Now, ψ_{sf}, ψ_{sb}, E_{sf}, and E_{sb} can be solved from (3), (4), (5), and (7) via a Newton-Raphson iteration method that is acceptable for physical, process-based compact modeling. Furthermore, the channel charge and current can be derived.

The main utility of the compact model is for circuit application. The generic DG model is useful for assessment of various device structures at both the device and circuit levels. More importantly, the model can be applied to gain insight into the effects of device parasitics (e.g., overlap capacitance) on device and circuit performances.

We first exemplify the model application with model-predicted I_{off} and I_{on} versus back-oxide thickness (t_{ob}) variation for 50 nm asymmetrical and symmetrical DG MOSFETs. As shown in Fig. 8, very different sensitivities are predicted for the same back-oxide thickness variation. The I_{off} of the asymmetrical DG device increases rapidly as back-oxide thickness increases due to less charge-coupling effect. In other words, the threshold voltage of the asymmetrical DG MOSFET has a stronger dependence on the back oxide thickness (t_{ob}). Continuously increasing t_{ob} will make the asymmetrical DG device like an FD SOI MOSFET, for which the high I_{off} becomes an issue. Conversely, the symmetrical DG device has lower I_{on} for thicker back oxide because of less back-channel current, as indicated in Fig. 9.

Using a 9-stage RO circuit for previous asymmetrical device, we also check the performance of DG and SG (with back-gate grounded) CMOS circuits, as demonstrated in Fig. 10. The DG MOSFET not only has better scalability and higher density, but also has dramatically superior performance over the SG counterpart due to higher carrier saturation velocity, implied by higher mobility. For low V_{dd}, the DG circuit performs even much better than the SG one because the dynamic threshold effect implied by low S

gives a higher gate overdrive (V_{GS} - V_T). Additionally, in weak inversion, near zero gate capacitance of the DG device due to charge neutrality is another great advantage over conventional bulk-like CMOS.

IV. Mixed-mode simulation

The mixed-mode simulation is another convenient tool for assessment of the developed device without the necessity of pre-simulation for LUT model generation or analytical model derivation. Its simulation time, depending on the size of the circuit, could be lengthy though.

Double-gate (DG) device can be employed either with two gates tied together or independently biased [13], as shown in Figs. 1 and 11. The separate biasing in DG device easily provides multiple threshold voltages, as demonstrated by a FinFET DG technology [14]. It can also be exploited to reduce the number of transistors for implementing logic functions [8].

For performance assessment of the two operation modes, we use the DG devices of L_{eff} = 50 nm with lightly doped ($N_{body} = 10^{15}$ cm^{-3}) thin silicon film (t_{Si} = 10 nm) and scaled oxide for front- and back-gate ($t_{oxf} = t_{oxb}$ = 2 nm). Metal gates with near-mid-gap work function are used to achieve the desired V_T with acceptable I_{off} ~ 100 nA/μm for V_{dd} of 1 V. Due to the inherent gate-to-gate coupling, the two configurations have very different characteristics. Fig. 12 shows MEDICI [15]- simulated nFET I_{DS} versus V_{GS} characteristics at V_{DS} = 0.05 and 1 V for double-gate (DG) (tied gates) mode and single-gate (SG) (back-gate biased at 0 V) mode. The DG mode provides near ideal subthreshold swing via strong gate-to-gate coupling, and higher I_{on} from the enhanced gate conduction from the strong coupling. The DG mode clearly outperforms the SG mode in I_{on} and I_{eff}, but note that the tied-gate case has almost twice higher effective gate capacitance than the SG case. The gate capacitance could become a significant factor in circuit performance, especially for gate dominant circuits. In addition, the independent gates of the SG mode provide design flexibility and hence can be beneficial for implementing logic functions.

V. Conclusions

Double-gate CMOS modeling techniques for device and circuit simulations, including look-up table modeling, compact device modeling, and mixed-mode simulation, were presented. Each of the modeling methodology has its unique features suitable for evaluating high performance DG CMOS circuits. We expect DG devices to be a very attractive choice for low-power technology due to their excellent performance.

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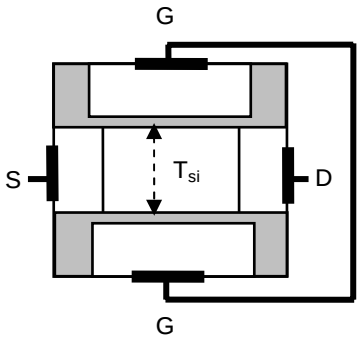

Fig. 1. Double-gate device structure with tied gates.

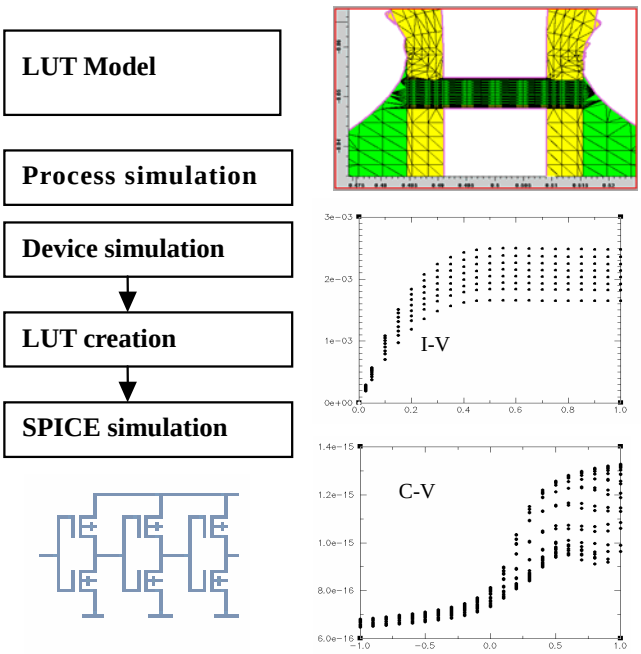

Fig. 2. Look-up table methodology.

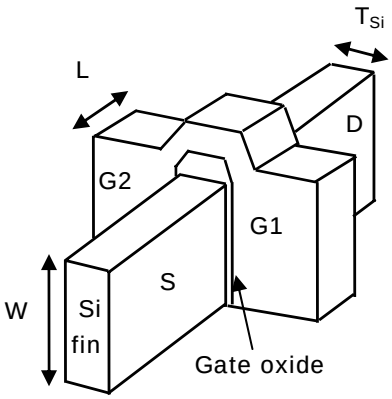

Fig. 3. FinFET device structure.

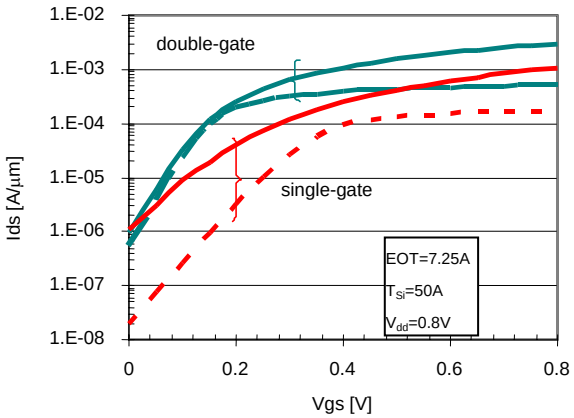

Fig. 4. I-V characteristics of FinFET (double-gate) and single-gate FDSOI device. with 18 nm gate length and 0.8 V power supply.

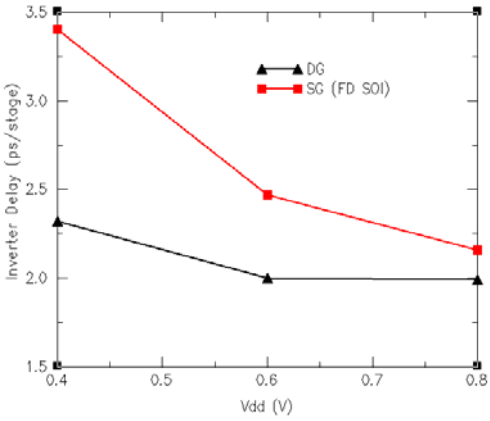

Fig. 5. Inverter delay for FinFET (DG) and FDSOI devices for different power supplies. Device width has been adjusted for I_{on} = 3 mA (Distributed gate resistance is not included).

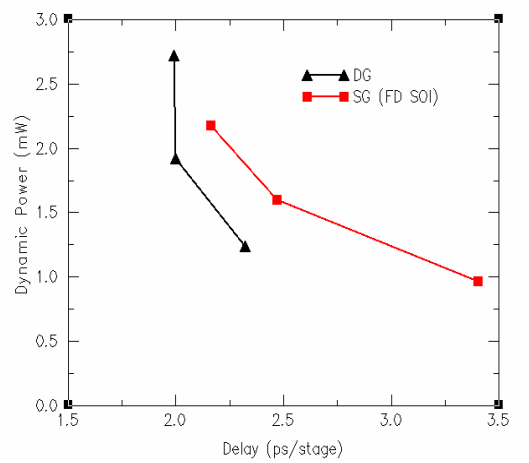

Fig. 6. Power-delay for inverter ring oscillator for 45nm technology with V_{dd} = 0.4, 0.6, and 0.8 V.

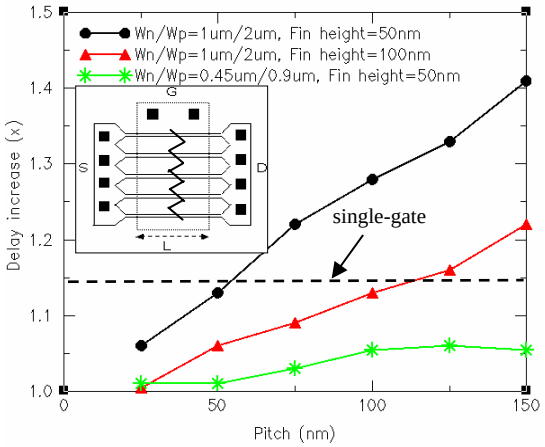

Fig. 7. Effect of distributed gate resistance on inverter delay for different device widths, fin heights, and pitch sizes. Insert shows inverter layout in FinFET implementation.

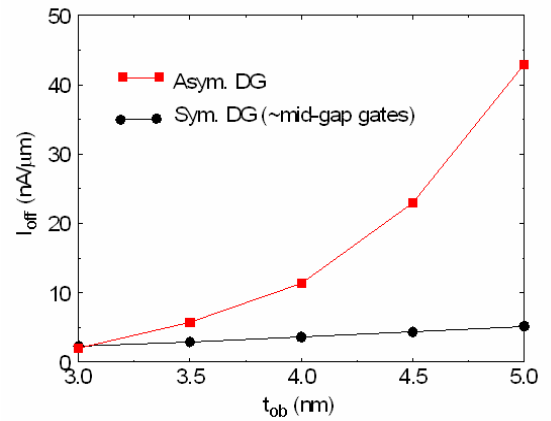

Fig. 8. Model-predicted I_{off} vs. back-oxide thickness variation.

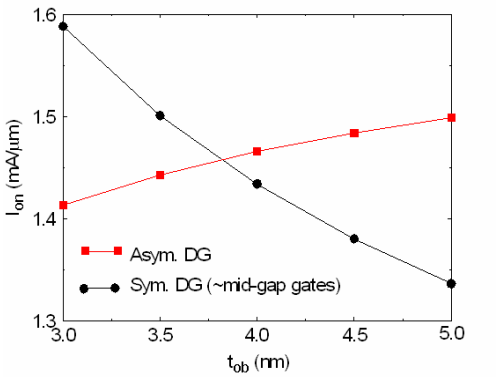

Fig. 9. Model-predicted I_{on} vs. back-oxide thickness variation.

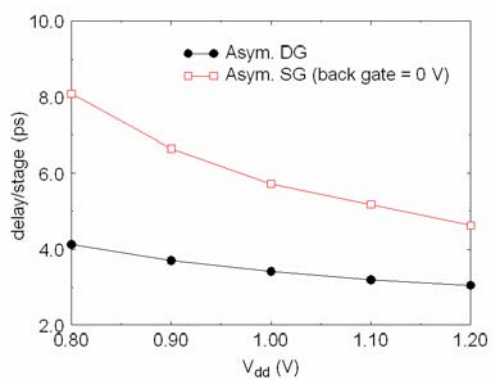

Fig. 10. Model-predicted inverter delay vs. V_{dd}.

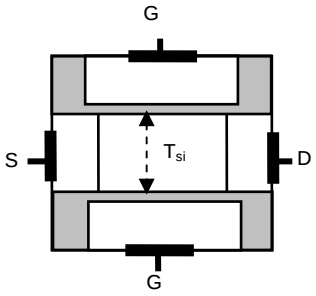

Fig. 11. Double-gate device structure with independent gates.

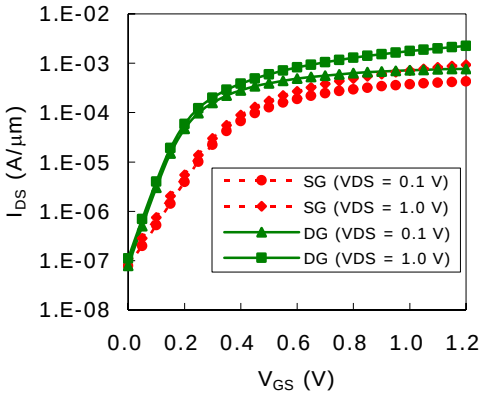

Fig. 12. MEDICI-simulated nFET I_{DS} – V_{GS} characteristics at V_{DS} = 0.05 and 1 V for double-gate (DG) (tied gates) and single-gate (SG) (back-gate biased at 0 V) modes.