國　立　宜　蘭　大　學

１０４學年度研究所碩士班考試入學

電子學試題

（電子工程學系碩士班）

准考證號碼：

《作答注意事項》

1.請先檢查准考證號碼、座位號碼及答案卷號碼是否相符。

2.考試時間：100 分鐘。

3.本試卷第 1 大題為選擇題:40 分，第 2~5 題為非選擇題:60 分，共計 100 分。

4.請將答案寫在答案卷上。

5.考試中禁止使用大哥大或其他通信設備。

6.考試後，請將試題卷及答案卷一併繳交。

7.本試卷採雙面影印，請勿漏答。

8.本考科所需電子計算機由本校提供。

1. Choose the correct answer for the following questions. (40%)

(1) A STC network has the transfer function: $T(s)=\dfrac{100}{s+1}$.

If the frequency is larger than the Corner Frequency, then the gain
(A) decreases 10 dB while the frequency increases 10 times
(B) decreases 20 dB while the frequency increases 10 times
(C) decreases 10 dB while the frequency increases 2 times
(D) decreases 20 B while the frequency increases 2 times.

(2) Compared with the *pn* junction under open circuit, which is correct about *pn* junction under reverse bias?
(A) Barrier of depletion region is decreased.
(B) Charge stored of depletion region is decreased.
(C) Width of depletion region is increased.
(D) Diffusion current is increased.

(3) For the ideal diode circuit shown in Fig.1, the voltage V_O =? (in V)
(A) –5 (B) –3 (C) 0 (D) 3

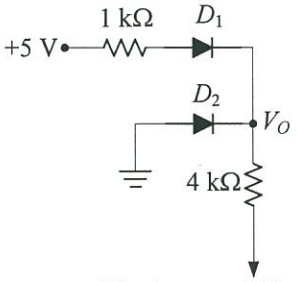
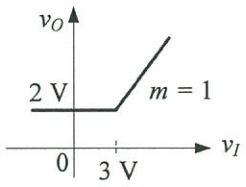
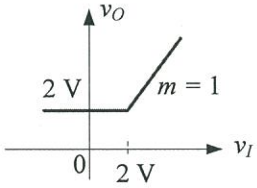
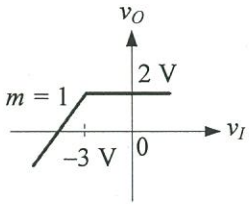


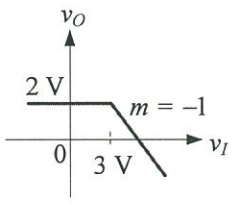
Fig.1

(4) For the ideal diode circuit shown in Fig.2, which is the correct voltage transfer characteristic? Assume *m* is the slope.

(A)


(B)


(C)


(D)


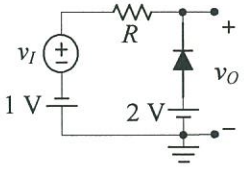


Fig.2

(5) What is the circuit shown in Fig.3, where v_O is the output?
(A) voltage doubler (B) filter
(C) limiting circuit (D) clamping circuit

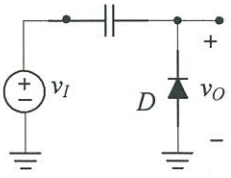


Fig.3

(6) Which is NOT correct about the Common Base amplifier?
(A) high voltage gain (B) good high frequency response
(C) high input resistance (D) high output resistance

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(7) An enhancement-type NMOS FET, with V_t = 1 V and k_n' = 25 μA/V^2, has its source terminal voltage = 2 V, drain terminal voltage = 3 V and a 2.5 V dc applied to the gate. What region does the device operate?
(A) Saturation (B) Cutoff (C) Triode (D) Active region

(8) The main merit of Wilson current mirror, shown in Fig.4, is
(A) high current gain (B) high voltage gain
(C) high input resistance (D) high output resistance.

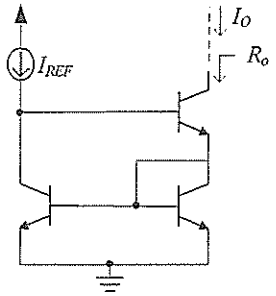

Fig.4

(9) For the opa circuit shown in Fig.5, the Q_1 and Q_2 are for
(A) current source (B) differential amplifier
(C) CS amplifier (D) frequency compensation.

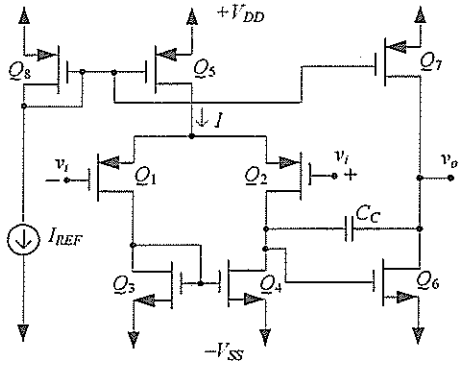

Fig.5

(10) Countinuing the above problem, the Q_8 and Q_5 are for
(A) current source (B) differential amplifier
(C) CS amplifier (D) frequency compensation.

2. For the circuit shown in Fig.6, assume the op amp to be ideal and let R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 2 kΩ, R_4 = 20 kΩ, find
(a) input resistance R_i
(b) voltage gain $A_v = v_x/v_I$
(c) output resistance R_o
(d) current gain i_4/i_1.
(20%)

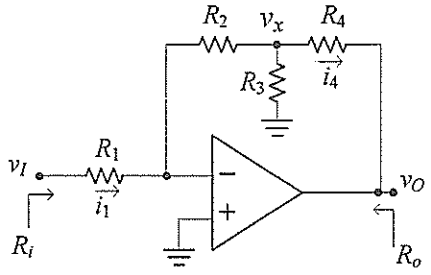

Fig.6

3. For the circuit shown in Fig.7, assume V_+ = +10.7 V, V_- = −10.7 V, R_C = 4 kΩ, R_E = 10 kΩ and BJT's β = 100.
(a) Find the current I_C.
(b) Find the largest value to which R_C can be raised while the transistor remains in the active mode.
(10%)

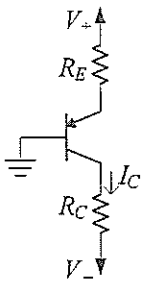

Fig.7

4. The amplifier shown in Fig.8 has the FET have $V_t = 1$ V, $k_n'(W/L) = 1$ mA/V^2 and $R_{sig} = 100$ kΩ, $R_G = 900$ kΩ, $R_D = R_L = 20$ kΩ, $R_S = 1$ kΩ, $I = 0.5$ mA. If the capacitors C_1, C_2 and C_S are ideal infinite,
(a) plot the small signal equivalent circuit for the circuit, find
(b) R_{in}
(c) $A_v = v_o/v_i$
(d) $G_v = v_o/v_{sig}$.
(20%)

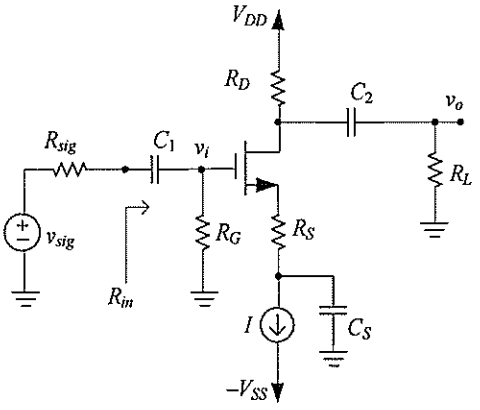

Fig.8

5. For the ideal opa circuit shown in Fig.9,
(a) what is the circuit's name?
(b) Assume that the op amp has ±12 V output saturation levels, $R_1 = 10$ kΩ, $R_2 = 40$ kΩ and $v_I = -5$ V, then the voltage of v_O =?
(10%)

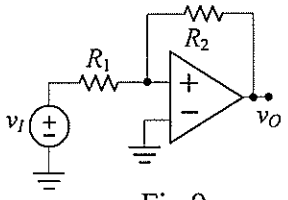

Fig.9